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DIFFERENTIAL PREAMPLIFIER HAVING BALANCED RESISTOR NETWORK

FIELD OF THE INVENTION

[001] The present invention relates to pre-amplifier circuits which are coupled to magneto-resistive ("MR") read/write heads utilized in hard disk drives ("HDDs").

BACKGROUND OF THE INVENTION

[002] The typical MR read/write head comprises a sensor or element that senses ambient magnetic fields at the head, causing a relative change in MR resistance. The change or variation produces a current variation that is received in the preamplifier. AC coupling, typically using capacitors, between the MR sensor and the amplifier stages prevents the amplifier input stages from being overloaded by DC voltages across the MR elements. A number of techniques have been developed to shorten DC settling transients and hence increase recovery times of the MR element. These techniques have been developed to increase the speed of the preamplifier. Conventional ac signal amplifiers use a transistor circuit coupled to the bases of the pre-amplifier transistor differential pairs to compensate and maintain the base currents at pre-determined levels. Disadvantageously, transistors are rarely perfectly matched, which gives rise to various offsets due to feedback current mismatches. A current mismatch results in a large input offset and bad switching recovery time due to the offset. Other arrangements that are designed to increase switching times and improve dynamic range use complex feedback loops. But feedback loops give rise to other problems such as increased recovery time and increased control circuit complexity. In contrast, the configuration of the present invention is not overly complex. Further, the performance of the preamplifier is improved as the present invention requires no trim or tuning for operation.

SUMMARY OF THE INVENTION

[003] The present invention is designed for AC signal pre-amplifiers, for use in among other things, the first stage of a MR sensor coupled preamplifier. The present invention reduces the current mismatch at the base of the first stage transistors, resulting in faster switching times by reducing input stage offset and, hence improving input dynamic range.

BRIEF DESCRIPTION OF THE DRAWINGS

[004] Figure 1 is a circuit diagram of an amplifier of the present invention; and

[005] Figure 2 is a plot of the control timing of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[006] When used with ac signal amplifiers, the present invention reduces current mismatch and results in faster switching times by reducing input stage offset. The present invention also improves input dynamic range. In order to optimize the performance of the present invention, no trim or tuning is required.

[007] Referring to Figure 1, MR sensor 140 is biased by a first current source 131 and a second current source 132 and is capacitively coupled to the preamplifier through first capacitor 121 and second capacitor 122. First capacitor 121 has a first terminal and second terminal, the second terminal being coupled at node 161 to the first circuit 101 of the preamplifier circuit. Second capacitor 122 has a first terminal and a second terminal, the second terminal being coupled at node 164 to the second circuit 102 of the preamplifier. The first terminal of the first capacitor 121 is cross-coupled to the second circuit 102 of the preamplifier circuit at node 163 and the first terminal of the second capacitor 122 is cross-coupled to the first circuit 101 of the preamplifier circuit at node 162. Base current compensation circuit 130 is coupled to the bases of a first amplifying transistor 141, a second amplifying transistor 142, a third amplifying transistor 143 and a fourth amplifying transistor 144. The base compensation circuit is comprised of a plurality of MOS transistors 180 driven by a reference current source 133. In operation the current value of current source 133 is basically a ratio of transistor 183 to

transistor 184 and by the ratio of transistor 181 to transistor 141, transistor 142, transistor 143 and transistor 144. Transistor 182 is cascoded to the base of 181 for sensing the correct value of base current. If the beta of transistor 141, transistor 142, transistor 143, transistor 144 and transistor 181 is same, MOS transistors 180 will supply the correct value of base current.

[008] The first capacitor 121 and second capacitor 122 prevent the DC component of the signal from entering the preamplifier. In normal operation, the impedance of capacitors 121 and 122 is very small in the signal band frequency. In such case, the circuit behaves like a single differential amplifier. But because the MR sensor requires bias, meaning the MR sensor has a voltage between its terminals, capacitors 121 and 122 need to charge until the differential pair base voltage is almost the same, Otherwise the circuit will not behave as a differential amplifier. Although this action is desired, it disadvantageously decreases the recovery time and hence speed of the entire circuit. What is desired is a configuration that retains the advantages of an AC coupled preamplifier circuit, but also is optimized for high speed operation.

[009] The present invention comprises the first circuit 101 feeding an output of the first stage of the preamplifier and a second circuit 102 coupled to the first circuit 101 and also feeding the output of the first stage of the preamplifier. The first circuit 101 is coupled to the second circuit 102 through the coupling of the collector of the third amplifying transistor 143 to the collector of the first amplifying transistor 141 and the coupling of the collector of fourth amplifying transistor 144 to the collector of the second amplifying transistor 142. DC voltage sources 114 and 115 provide a cascade connect.

[010] A current loop 171 within the first circuit 101 further comprises a first resistor 110 with a first terminal and second terminal, a first transistor switch 103 with an input and output and control lead, and a second resistor 111 with a first terminal and second terminal, the first resistor 110 and second resistor 111 comprising a pair of balanced resistors. The second terminal of the first resistor 110 is coupled to the input of the first transistor switch 103, the second terminal of the second resistor 111 is coupled to the output of the transistor switch 103, the first terminal of the first resistor 110 and the first terminal of the second resistor 111 are coupled to the bases of a first differential pair of transistors 141 and 142, respectively, with a second transistor switch 104 being

coupled across the bases of the first differential pair of transistors 141 and 142 at nodes 151 and 152.

[011] In addition, the present invention comprises a second current loop 172 within the second circuit 102. The second current loop comprising a third resistor 112 with a first terminal and second terminal, a third transistor switch 105 with an input and output, and a fourth resistor 113 with a first terminal and second terminal, the third and fourth resistors also comprising a pair of balanced resistors. These switches are on during normal read mode, when differential pairs 101 and 102 are active. The second terminal of the third resistor 112 is coupled to the input of the third transistor switch 105, the second terminal of the fourth resistor 113 is coupled to the output of the third transistor switch 105, the first terminal of the third resistor 112 and the first terminal of the fourth resistor 113 are coupled across the bases of a differential pair of transistors 143 and 144 with a fourth transistor switch 106 being coupled across nodes 153 and 154.

[012] Referring to the time domain waveform plot of Figure 2, upon a mode change, transistor switches 104 and 106 turn on to charge up input capacitors 121 and 122 respectively. Without the current loops 171 and 172, and due to process or other variations, the time-based current provided by base current compensation circuit 130 to the amplifying transistors 141, 142, 143 and 144 are equal. As a result, an offset develops due to the differential in current between each side of the amplifying circuits coupled to the MR sensor. The input offset results in slow recovery times and poor input dynamic range.

[013] Figure 2, illustrates the control timing of switches 104 and 106. As seen in the plot of the control timing of Figure 2, switches 104 and 106 are on during a very short period of time at switching due to the fast charge up of capacitors 121 and 122. The loop circuits 171 and 172 of the present invention operate to reduce the current mismatches between the two circuits 101 and 102. As a result the preamplifier has better recovery time and better input offset. Improving the input offset results in better input dynamic range.

[014] The innovative teachings of the present invention are described with particular reference to its use in MR coupled preamplifier circuits. However, it should be understood and appreciated by those skilled in the art that these embodiments provide

only one example of the many advantageous uses and innovative teachings herein. Various alterations, modifications and substitutions can be made to the disclosed invention without departing in any way from the spirit and scope of the invention.